

TECHNICAL WHITE PAPER

AION ENTERPRISE BROADCAST

VERSION B / ST 2110 TIMING + EIGHT-CHANNEL OVERLAY

GPS-Disciplined PTP Grandmaster

Protected UHD Media Paths and Facility Timecode Distribution



PRECISION TIMING / PROTECTED MEDIA / INDEPENDENT CHANNELS

01 / EXECUTIVE OVERVIEW

Timing meets media infrastructure

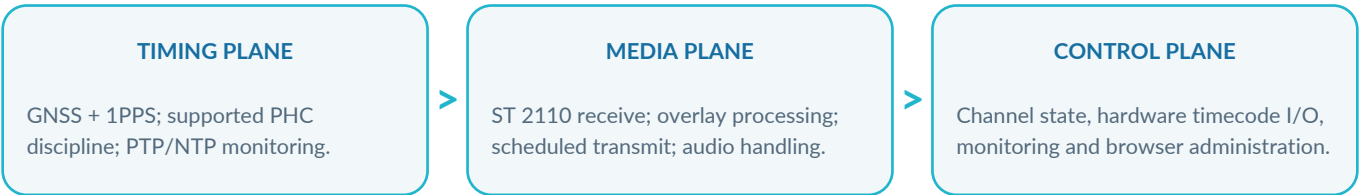
A facility-focused master clock, eight independent video paths, and a unified operational control plane.

Aion Enterprise Broadcast (Version B) is the pre-release broadcast member of the Aion product family. It combines a proposed GPS-disciplined SMPTE ST 2059-2 PTP grandmaster, a DeckLink IP 100G media interface, independently controlled overlay channels, and legacy/network timecode distribution in a single managed 2U platform.

DESIGN PRINCIPLE

One coherent time reference. Eight independently configured media pipelines. The common clock provides temporal consistency; each channel retains its own overlay state, routing, frame format and timecode presentation.

Three operating planes



The target hardware and DeckLink IP 100G specifications support the concept of eight concurrent Ultra HD paths on Linux. However, the supplied C++ source is a **single-path DeckLink passthrough/overlay implementation**. Eight-channel instantiation, IP-card integration and aggregate performance remain to be developed and validated.

EXISTING TECHNOLOGY

The supplied module contains DeckLink I/O callbacks, Cairo/Pango overlay rendering, BGRA frame conversion, LTC-audio generation, UDP control and latency telemetry.

ENTERPRISE DEVELOPMENT

Eight configured path instances, PTP-aligned media time, ST 2110-specific routing/ANC behavior, per-path lifecycle control and full-load validation.

Product family: Enterprise Academic (A) addresses campus and signage orchestration; Enterprise Broadcast (B) addresses professional ST 2110 timing, video overlays and facility timecode distribution. The variants share timing lineage but have different media and hardware specifications.

02 / SOURCE REVIEW

What the code establishes

Findings are based on the supplied tc-overlay-src C++ archive, not on eight-channel benchmark results.

Component	What is present in the current source
InputLoopThrough.cpp	Single configured DeckLink input/output, global Cairo overlay, UDP handler and audio manager.
CairoTextOverlay.cpp	Cairo/Pango text graphics; style, placement, background, border and reusable cached surfaces.
Bgra32VideoFrame.cpp	8-bit BGRA working-frame wrapper and DeckLink format conversion helpers.
AudioTrackManager.cpp	LTC waveform generation/insertion into a selected audio track.
DeckLinkOutputDevice.cpp	Scheduled video/audio playback, reference-lock monitoring and latency reporting.
UdpHandler.cpp	Timecode commands, configuration, video format information and telemetry.

MATERIAL DIFFERENCE

The original white paper described eight independent UHD overlay threads as if their aggregate cost were established. In the reviewed module, overlay text generation is region-local, but the video conversion and output-frame creation operate on **full video frames**. CPU and memory bandwidth therefore require separate proof.

The precise portability boundary

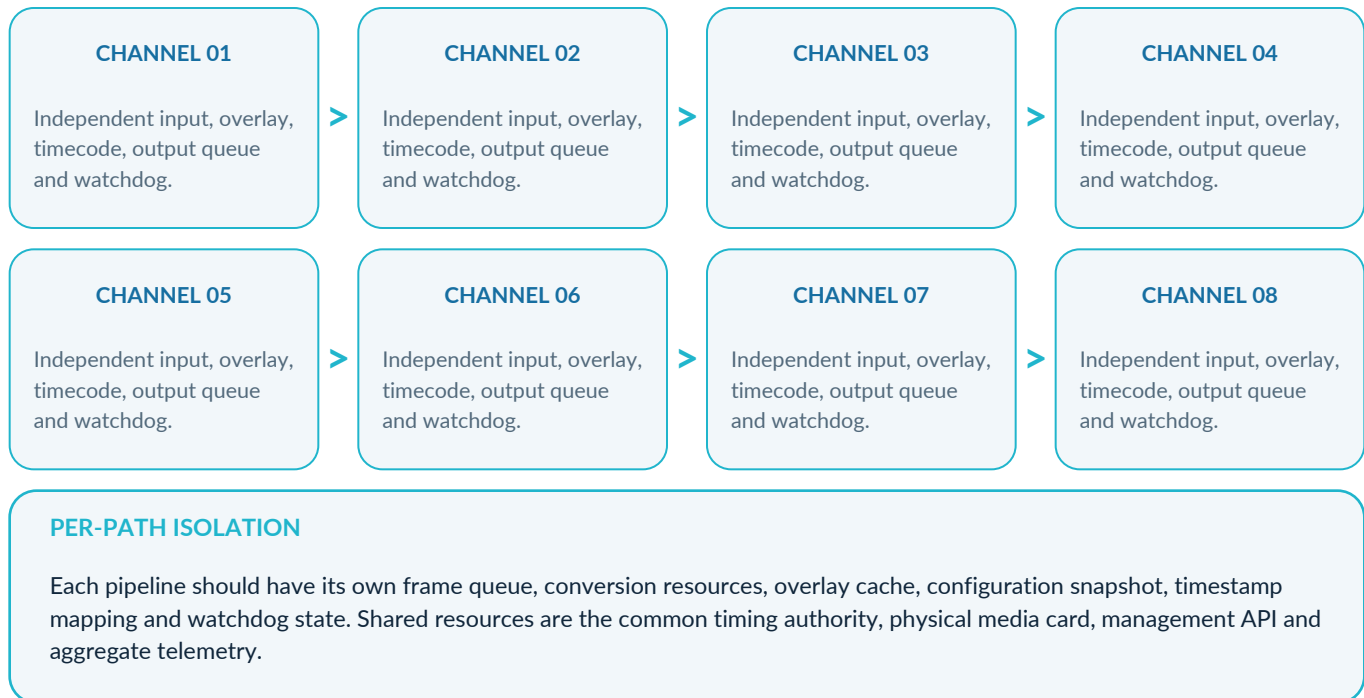
The current executable uses global handlers and a fixed UDP listener/transmitter configuration. Multiple processes can provide address-space isolation, but require unique control ports, deterministic channel/device mapping and central supervision. A multi-instance in-process design instead requires the global state to become per-channel state, with thread-safe shared services.

The CMake configuration also references additional sources and desktop preview dependencies. A headless Enterprise build profile and a reproducible IP-card build/test environment must be defined before integration is considered complete.

03 / EIGHT-CHANNEL MODEL

Eight independent pipelines

A scaled-out design rooted in the current passthrough program, not eight copies sharing a single global state.



Preferred software construction

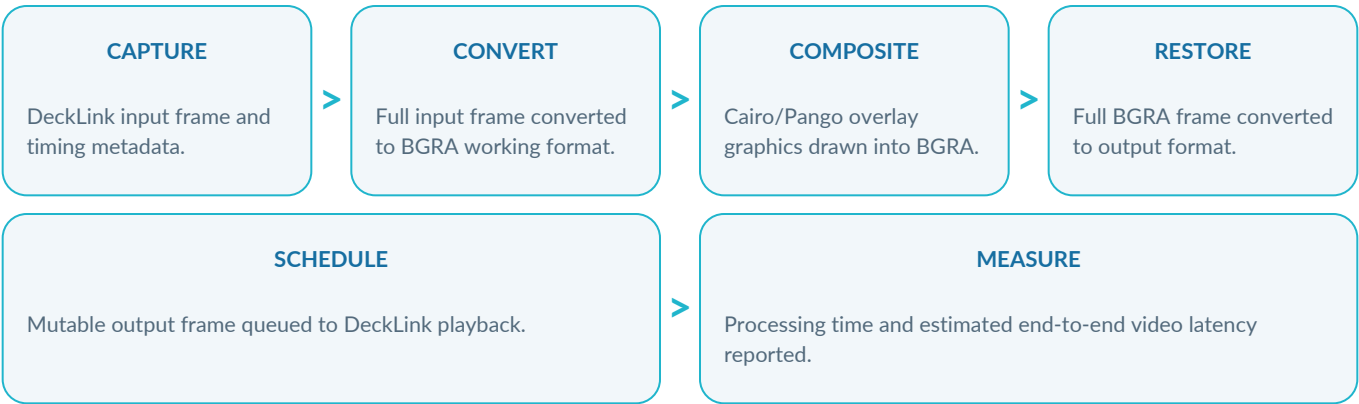
Build a **ChannelContext** abstraction around input, compositor, output, audio association and monitoring. A supervising service creates up to eight contexts and binds each to the appropriate DeckLink IP senders/receivers. An alternate first milestone is eight isolated workers with unique configuration and UDP endpoints. Neither model should rely on the existing process-global singletons.

The number of independent DeckLink SDK logical devices and routing semantics available per IP 100G card must be confirmed on the installed Linux driver/SDK combination, not inferred solely from eight published channels.

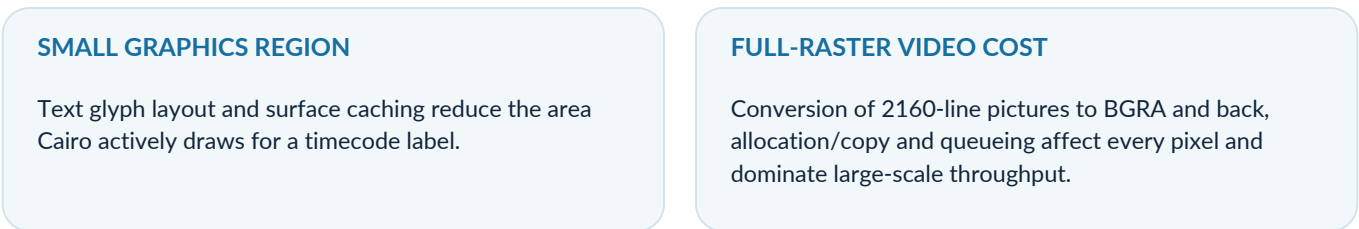
04 / OVERLAY DATA PATH

Where the pixels travel

The current module already provides a functioning overlay path; its full-frame conversions are central to capacity planning.



Two distinct costs



At 3840 x 2160, one 8-bit BGRA buffer is approximately **33.2 MB**. At 60 fps, traversing that buffer once is roughly **2.0 GB/s per channel**, before other reads, writes, conversion or buffering. Eight instances amplify these demands. The real pipeline may traverse the frame multiple times.

QUALITY CONSIDERATION

The working buffer is 8-bit BGRA while the broadcast I/O path may carry 10-bit 4:2:2. A 10-bit to 8-bit to 10-bit conversion path is **not inherently bit-transparent**. Enterprise development should validate picture fidelity and evaluate a higher-precision or overlay-only compositor for critical workflows.

05 / STREAM BANDWIDTH

Plan for protected 100G

The DeckLink IP 100G supports eight UHD p60 channels on Linux; protected capacity is assessed per 100G network leg.

Format	One stream, active picture	Eight streams, active picture
1080p60 / 10-bit 4:2:2	~2.49 Gb/s	~19.9 Gb/s
2160p30 / 10-bit 4:2:2	~4.98 Gb/s	~39.8 Gb/s
2160p60 / 10-bit 4:2:2	~9.95 Gb/s	~79.6 Gb/s
2160p60 / 8-bit 4:2:2	~7.96 Gb/s	~63.7 Gb/s

Values are active-picture payload estimates computed as width x height x frames/second x effective bits/pixel. They exclude packet transport overhead, timing/audio/ANC essences, switching and operational headroom. Actual flows must be assessed using negotiated transport parameters and monitored line rates.

The IP10 distinction

Blackmagic documents IP10 as a way to fit UHD 59.94/60 into **10GbE per channel**. It is not correct to state that 8 x UHD60 intrinsically requires IP10 solely because the deck has a 100G uplink. Codec requirements depend on per-stream link limits, end-to-end compatibility, bitrate planning and the configured ST 2110 environment.

PROTECTED NETWORK MATHEMATICS

In a SMPTE 2022-7 A/B deployment, the primary and secondary links carry the redundant media flows. **Two 100G ports are not a single protected 200G payload pipe.** The traffic on each independent network must fit the usable capacity of one link, including operational margin.

Blackmagic currently publishes up to 2160p60 for DeckLink IP 100G. The old paper's 2160p120 specification should be removed unless a separately supported transport/media path is demonstrated. Its PCIe interface is Gen4 x8, even when plugged into a larger Gen5 slot.

06 / COMPUTE AND MEMORY

Eight paths need evidence

The processor selection must follow measured end-to-end throughput, not overlay glyph size alone.

Load component	What must be measured
Color conversion	CPU cycles or hardware offload, 10-bit handling and picture fidelity.
Frame allocation	Memory lifetime, queue depth, buffer reuse and allocation rate.
Memory bandwidth	Read/write traffic per processed frame across eight channels.
PCIe Gen4 x8	Actual DMA ingress/egress and practical bidirectional headroom.
Video scheduling	Per-channel deadline misses, queued frames, drops, and output latency.
Mixed workloads	Overlay plus embedded LTC, PTP, NMOS, web API and telemetry.
Thermals	Sustained i9-14900K frequency, power cap and cooling stability.

Hardware direction from the original design

The proposed W680 platform, ECC UDIMM memory, i9-14900K processor, redundant 500W modules, management BMC and 2U thermal system remain reasonable **engineering candidates**. The original paper's claim of ample CPU headroom for eight UHD60 paths cannot yet be substantiated from the supplied code alone.

The overlay pipeline should offer at least two performance modes: direct passthrough when an overlay is disabled, and a validated video-compositing path when active. The current disabled-overlay branch still performs conversion work and is therefore an optimization target.

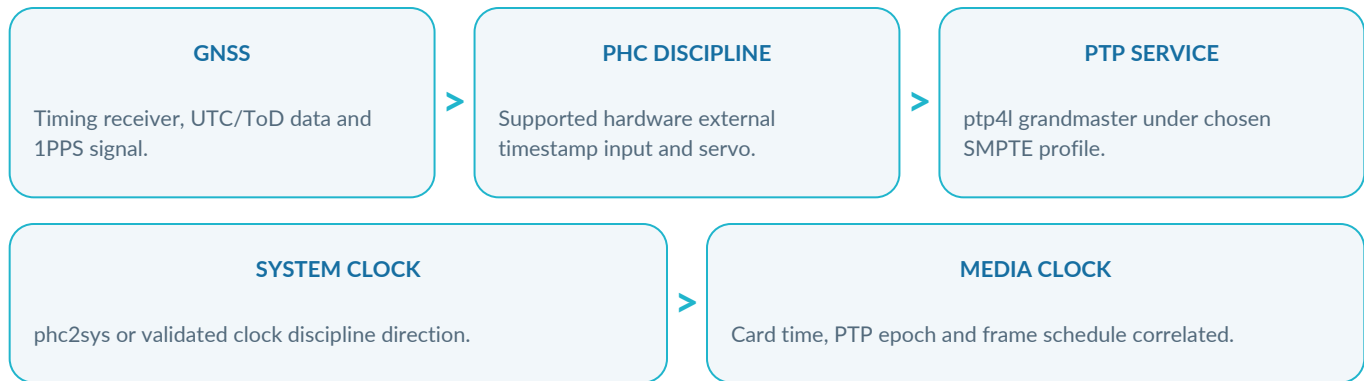
ACCEPTANCE GATE

Before committing to a fixed BOM, run 1, 2, 4 and 8-channel soak tests at HD, UHD30 and UHD60, recording average/p99 processing time, memory bandwidth, scheduling errors, picture fidelity and reference stability.

07 / TIMING CHAIN

GPS to grandmaster

A reference-grade PTP grandmaster requires a proven path from hardware 1PPS to the PTP hardware clock.



The original white paper described gpsd SHM as if ptp4l directly used it as a GPS refclock. That is not a generally valid linuxptp grandmaster implementation. The design should instead specify an actual hardware PPS-to-PHC discipline mechanism, such as **ts2phc on a supported NIC**, or another measured and supported architecture.

TAI / UTC and holdover

- GNSS time-of-day, leap-second status and the TAI-UTC offset must be supplied and validated through the selected receiver and synchronization stack. Ordinary NMEA UTC sentences alone do not justify an automatic leap-second claim.
- GPS reference loss triggers the appropriate PTP clock-class/traceability response. Holdover duration depends on the oscillator, temperature and characterized drift, not just software uptime.
- SMPTE ST 2059-2 profile configuration, domain numbers, priority and boundary/transparent-clock network behavior require site validation.

COMMON REFERENCE / DISTINCT TIMECODE

All overlays and timecode generators may derive coherent base time from the grandmaster, while channels apply independent frame rates, offsets or operational time representations. Displaying different values does not imply separate physical reference clocks.

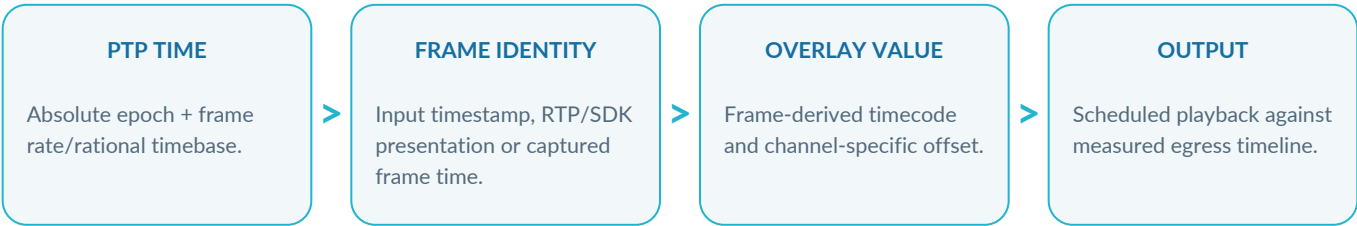
08 / MEDIA CLOCK COHERENCE

Align each frame to time

Sharing the server clock is necessary, but does not alone make overlay graphics frame-accurate at each ST 2110 output.

Required correlation

For each received frame, the Enterprise media layer should identify the frame's capture/presentation timing, correlate it with the PTP-aligned media timeline, calculate the intended timecode at that event time, then schedule the outgoing frame with validated timing semantics.



The supplied single-path C++ code increments an atomic frame counter and updates the UDP timecode engine on processed frames. That is an operational implementation for the current application, not evidence that the timestamp on every Enterprise ST 2110 frame is already PTP-aligned.

FRAME RATE

Use rational rates such as 30000/1001 and 60000/1001 where appropriate; verify drop-frame rules and midnight rollover.

PIPELINE LATENCY

Track frame-arrival, scheduling and completion timing. The code's additional 2.5-frame hardware-delay allowance is an estimate, not an end-to-end physical measurement.

SYNC TARGET

Qualify full-path timing against an external PTP-aware reference and real media equipment. Avoid claiming sub-microsecond *overlay presentation* merely because the grandmaster itself is accurate within that range.

09 / TIME CODE DISTRIBUTION

A shared timing hub

Retain the six distribution families described in the Broadcast reference, while separating source-proven code from Enterprise additions.

Distribution	Proposed Broadcast behavior / evidence
PTP grandmaster	GPS-disciplined timing service, dual timing-plane NICs and SMPTE ST 2059-2 profile; site-specific validation required.
Embedded LTC in ST 2110-30	Per-channel LTC audio essence, associated with each media path; existing code generates LTC into a selected track, not yet demonstrated on eight IP flows.
Hardware LTC	Dedicated generator and reader subprocessors from the Aion timing product line, subject to final integration.
IRIG A/B	Selectable hardware generator and reader, mutually exclusive with LTC on their respective shared I/O channels.
Art-Net timecode	Management-plane timecode distribution based on backend timing engine.
TSL-UMD and UDP	Network timecode/status delivery and custom integrations with an Enterprise extension of the existing command schema.

All mechanisms should be explicit about whether they convey authoritative time, offset timecode, audio-encoded LTC, or control/status. An independent offset changes a presented value, not the rate or stability of the underlying clock.

10 / AUDIO, ANC & METADATA

Preserve the whole program

ST 2110 separates essence flows; a video overlay solution must explicitly account for audio, timecode and ancillary continuity.

Audio/LTC implementation

The current code has an audio manager that inserts LTC into a selected track of the captured/output audio packet. Enterprise development must bind audio essences to the correct media channel, establish stable sample alignment and validate the expected ST 2110-30 routing, sampling and receiver compatibility.

Ancillary and metadata handling

The current BGRA frame class returns E_NOTIMPL for timecode and ancillary-data access. Processed frames are rebuilt as new video frames. Thus, **preservation of ST 2110-40 ancillary content, captions, RP188, HDR signaling and other metadata cannot be claimed from the supplied source.**

REQUIRED ENGINEERING WORK

Explicitly pass through, remap or regenerate the relevant ANC metadata using the applicable DeckLink SDK interfaces; check captions, HDR/SDR colorimetry, frame identifiers and output metadata on each configured format.

Overlay precision

The compositor currently uses an 8-bit BGRA intermediate representation. Validate color-range mapping, 10-bit YUV conversions, Rec.709/Rec.2020 behavior, alpha blending and resulting overlay quality. Use a higher-precision compositing strategy when necessary for picture-preserving workflows.

ProRes and DNx codecs appear in the DeckLink vendor media-format ecosystem, but should not be presented as simultaneous live ST 2110 essence compression modes without a qualified application-specific workflow.

11 / HARDWARE PLATFORM

Designed for the rack

The original mechanical concept is retained, with capacity and integration claims explicitly qualified.



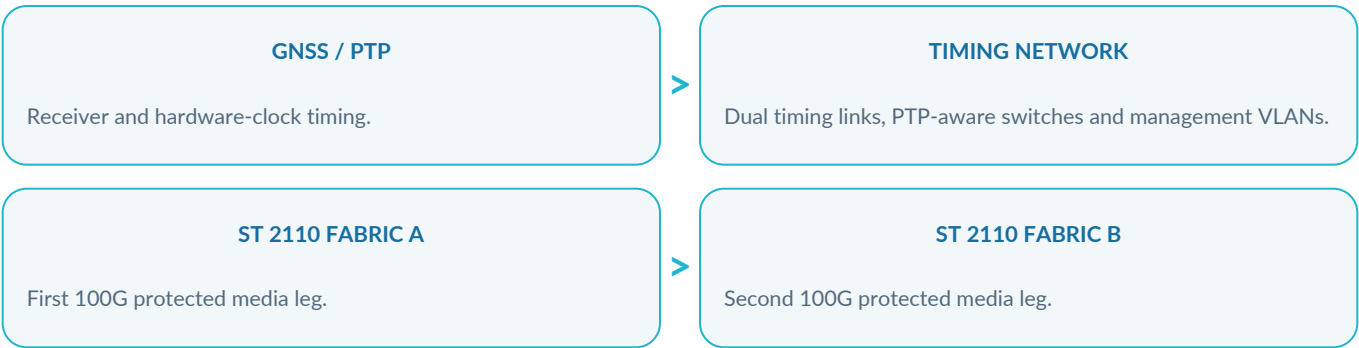
Aion Enterprise Broadcast front-panel enclosure concept. Final hardware and front-panel instrumentation are subject to engineering validation.

Subsystem	Proposed configuration
Main compute	Intel W680 micro-ATX server-class platform; Intel Core i9-14900K candidate; DDR5 ECC UDIMM.
Management	ASPEED AST2600 BMC/IPMI on selected board; separate remote-management access.
Media I/O	DeckLink IP 100G, PCIe Gen4 x8, dual QSFP28 100G ports, vendor-rated up to 8 UHD60 channels on Linux.
Timing I/O	Hardware-timestamped NICs; supported external PPS/PHC discipline, validated for selected board and interface.
Power	Redundant 2 x 500W hot-swap power modules (concept target).
Thermal	2U-compatible Dynatron L35 liquid cooling candidate; sustained power/temperature testing required.
Front panel	Independent compact monitoring processor and 3.5-inch display proposed.

12 / PROTECTED MEDIA NETWORK

A and B remain separate

The PTP and management topology should be designed independently of the redundant video fabric.



Topology and bandwidth constraints

- Each 100G fabric must carry its required stream set independently; SMPTE 2022-7 duplicates protected essences across the network legs.
- ST 2110 multicast, IGMP handling, QoS, PTP awareness, NMOS routing and stream receiver compatibility require acceptance testing at the target facility.
- PTP on dual NICs may represent links within one domain or interfaces in separately engineered timing networks. NIC availability alone does not create automatically fail-safe grandmaster or PTP domain redundancy.

The media-card SDK's ST 2110, 2022-7 and NMOS capabilities are manufacturer-documented. Aion's Enterprise configuration, monitoring and policy integration remain separate software deliverables.

13 / BACKEND AND OPERATIONS

Supervise every channel

A web-based operator interface should expose the timing chain, media pipelines, hardware endpoints and operational faults.

GRANDMASTER VIEW

GNSS fix/PPS status; PHC lock; PTP master state; traceability; UTC offset; current domain; holdover alarms.

MEDIA HEALTH VIEW

Per-channel input/output format, source ID, route, frame queue, overlay state, missed deadlines and sender/receiver status.

TIMECODE I/O

Hardware LTC and IRIG assignment, source selection, channel offsets, Art-Net, TSL-UMD, UDP distribution.

SYSTEM HEALTH

CPU, RAM, NVMe, thermal state, NIC links, process restarts, power modules and diagnostic display health.

Isolation and recovery

Eight independent workers or contexts should support controlled restart of a failed channel without forcing the entire timing authority offline. A supervisor should detect stalled capture, delayed playback, failed format reconfiguration and degraded external reference states.

Web UI changes need versioned per-channel configuration and transactional application. The C++ module's UDP command scheme provides an existing interface example; Enterprise should secure, identify and namespace each channel, preventing port collisions and unintended cross-control.

PTP IS A SHARED INFRASTRUCTURE SERVICE

A channel overlay failure must not restart or perturb the GPS/PTP master. Timing processes should have independent service supervision, priority and failure boundaries from the media compositor.

14 / DEPLOYMENT & HOLDOVER

Plan the failure modes

Network engineers and systems integrators need explicit assumptions for every critical dependency.

Failure or change	Expected response / validation objective
GNSS antenna loss	Class/status transitions to documented holdover; notify immediately; preserve current offset/traceability history.
PTP boundary switch loss	Clients and media equipment change clock state according to approved redundancy and BMCA plan.
100G network leg loss	2022-7 protected receivers remain stable if the surviving fabric carries the full media set.
Media channel stall	Isolate, alarm and restart an affected pipeline without disturbing unrelated outputs.
Overlay rendering fault	Defined unmodified passthrough or safe fallback, with appropriate program and metadata preservation.
Power module failure	Continue operation on the remaining module and report health; verify under sustained UHD workload.
Host OS restart	Out-of-band management survives independently; startup restores saved configuration and measured clock states.

Every site requires GPS antenna exposure, lightning protection, suitable low-loss coax, correct PPS input design, rack airflow, BMC segregation, software change control and deliberate PTP domain planning. The design should not promise a fixed holdover duration until oscillator stability has been characterized.

15 / IMPLEMENTATION STATUS

Proven lineage vs new work

Aion Broadcast combines technology with actual product lineage and an Enterprise integration program not yet completed.

Source-supported foundation	Enterprise-specific remaining work
DeckLink video capture/playback, current single-path scheduling.	Bind and supervise eight simultaneous DeckLink IP 100G paths.
Cairo/Pango overlay, cache and formatting.	Eight-channel throughput, image fidelity and memory optimization.
LTC audio generation/insertion in current workflow.	ST 2110-30 LTC per-channel routing and A/V/sample alignment.
Timecode commands, formats and UDP telemetry.	Namespace and secure per-channel controls and live routing.
Video latency timing and reference monitoring.	PTP-correlated frame identity and complete measured egress latency.
Earlier Aion timing / GPS / linuxptp code lineage.	Verified 1PPS-to-PHC discipline, leap data and failover behavior.
2U server design and front panel concepts.	Finalized BOM, wiring, thermal tests and certification.

STATUS LANGUAGE

The product supports **eight-channel UHD as an architectural target** based on the selected media card's vendor specification. Do not describe eight fully validated proprietary overlay modules, or their performance/accuracy, as shipped capabilities before qualification.

16 / VALIDATION MATRIX

The eight-channel qualification plan

Engineering acceptance must be repeatable on a known hardware/driver/SDK stack.

Test	Required evidence
Device discovery / routing	8 input-to-output media pairs, correct NMOS mappings and independent reconfiguration.
Format sweep	1080p60, UHD30, UHD59.94/60; supported pixel formats and codec/flow paths.
Performance scaling	1 / 2 / 4 / 8 channels, overlay on/off, CPU %, RSS, bandwidth, thermal and queue depth.
Timing correlation	PTP offset, input timestamps, scheduled output, measured video phase and timecode correctness.
Image integrity	10-bit preservation strategy; Rec.709/2020; HDR and SDR color reproduction.
Audio & ANC	LTC level and polarity, ST 2110-30 associations, ST 2110-40 content and captions.
2022-7 protection	Loss/recovery of either link under full traffic; packet/path monitoring.
Long-duration soak	At least 24h full-load tests plus targeted stability/failure-injection campaigns.
Reference faults	GPS loss, leap offset management, PTP domain conflict, holdover and recovery.

Record test results as measured values, not extrapolated claims. A production release should document validated maximum channel count by resolution, frame rate, pixel format, overlay mode and ancillary/audio configuration.

17 / REVISED SPECIFICATION

Enterprise Broadcast at a glance

Design targets unless specifically attributed to vendor-confirmed hardware capabilities.

Category	Current Broadcast concept
Purpose	GPS-disciplined PTP grandmaster and eight-channel ST 2110 live overlay/timecode hub.
Hardware	2U W680/i9 candidate, ECC UDIMM, IPMI BMC, redundant PSUs, independent front diagnostics.
Media card	DeckLink IP 100G; PCIe Gen4 x8; 2 x 100G QSFP28 (protected links).
Media path	Up to 8 UHD60 capture/playback paths supported by card on Linux; overlay performance not yet qualified.
Overlay	Cairo/Pango text compositor with full-frame BGRA conversion in existing single-path implementation.
Clock	Timing-grade GNSS + hardware 1PPS; PTPv2 / SMPTE ST 2059-2 design, discipline topology to be validated.
Timecode	Proposed 8 software channel states; LTC/IRIG subprocessor hardware; Art-Net, TSL-UMD and UDP.
IP media	ST 2110-20/-21/-30/-40, SMPTE 2022-7 and NMOS support derived from selected card; app integration pending.
Operating system	Debian Linux target; production headless service and reproducible build required.
Presentation/ANC	10-bit quality and metadata passthrough need explicit engineering work.
Commercial status	Pre-release design; deployments and integration planned per facility, quotation on request.

18 / REFERENCES & NEXT STEPS

Evidence-led engineering

The Broadcast system can be built incrementally while protecting the capabilities and limits of the existing Aion platform.

Recommended next engineering sequence

- 1. Establish a headless, reproducible single-channel build against DeckLink IP 100G on Linux.
- 2. Confirm ST 2110 capture/playback routing, protected A/B link behavior, reference timing and metadata.
- 3. Extract per-channel state into a ChannelContext with documented interfaces and lifecycle control.
- 4. Optimize the BGRA compositing path or adopt a measured high-precision overlay-only strategy.
- 5. Correlate timecode and scheduled playback to PTP-aligned frame timestamps.
- 6. Scale through two, four and eight channels, and publish qualified performance envelopes.

Primary technical references

Aion source materials: Aion Enterprise Technical Architecture & Design Reference (2025); Aion Enterprise Product Brochure (2026); tc-overlay-src C++ archive provided for this review.

Manufacturer documentation: Blackmagic DeckLink IP 100G technical specifications and DeckLink IP product documentation, including 8 UHD60 Linux paths, two 100G links, IP10 behavior and supported SMPTE standards.

Time synchronization: linuxptp documentation for ts2phc, ptp4l and phc2sys. The final PPS/PHC architecture must match verified hardware capabilities.

Public links:

blackmagicdesign.com/products/decklinkip/techspecs

blackmagicdesign.com/products/decklinkip

linuxptp.org/documentation/ts2phc/

linuxptp.org/documentation/phc2sys/

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